US-PAT-NO: 5388328

DOCUMENT-IDENTIFIER: US 5388328 A

TITLE: Process for fabricating an interconnected

multilayer board

DATE-ISSUED: February 14, 1995

CITY	STATE	ZIP
OIII	011111	
Toride	N/A	N/A
Walashama	NT / 7N	N/A
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Yokohama	N/A	N/A
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Hiratsuka	N/A	N/A
Yokohama	N/A	N/A
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E CIII	UIAIL	711
Tokyo	N/A	N/A
	Yokohama Yokohama Hiratsuka Yokohama Yokohama Yokohama Yokohama Yokohama Yokohama CITY	Toride N/A Yokohama N/A Yokohama N/A Yokohama N/A Hiratsuka N/A Yokohama N/A Yokohama N/A Yokohama N/A Yokohama N/A Yokohama N/A Yokohama N/A  Yokohama N/A  Yokohama N/A  Yokohama N/A

APPL-NO: 8/ 187546

DATE FILED: January 28, 1994

PARENT-CASE:

CROSS REFERENCE TO RELATED APPLICATIONS This application is

a divisional of

application Ser. No. 08/037,543, filed on Mar. 22, 1993,

now U.S. Pat. No.

5,300,735, issued on Apr. 5, 1994, which application is a continuation of application Ser. No. 07/672,117, filed on Mar. 19, 1991, (now abandoned).

## FOREIGN-APPL-PRIORITY-DATA:

FOREIGN-PRIORITY:

FOREIGN-PRIORITY-APPL-NO: JP 2-69259

FOREIGN-PRIORITY-APPL-DATE: March 19, 1990

INT-CL: [6] H05K003/10

US-CL-ISSUED: 29/852,29/830 ,156/902 ,174/267 ,428/901

US-CL-CURRENT: 29/852,174/267 ,216/20 ,29/830 ,428/901

FIELD-OF-SEARCH: 428/901;29/829 ;29/846 ;29/830 ;29/825 ;29/852 ;156/902 ;174/267

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## REF-CITED:

PAT-NO	ISSUE-DATE	PATENTEE-NAME	
US-CL			
4685033	August 1987	Inoue	N/A
4970106	November 1990	DiStefano et al.	N/A
5082718	January 1992	Chantraine et al.	N/A
5118385	June 1992	Kumar et al.	N/A

U.S. PATENT DOCUMENTS

## OTHER PUBLICATIONS

IBM Tech Discl Bull vol. 9 No. 10 Mar. 1967 pp. 1258-1259 by C. G. Lester et al.

IBM Tech Discl Bull vol. 11 No. 8 Jan. 1969 p. 962.

IBM Tech Discl Bull vol. 21 No. 4 Sep. 1978 pp. 1396-1397 by D. R. Tomsa et al.

ART-UNIT: 326

PRIMARY-EXAMINER: Arbes; Carl J.

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus

## ABSTRACT:

A process for the fabrication of an interconnected

multilayer board involves the steps of forming a metallic under-conductive layer on a base substrate, forming a windowed resist layer on the metallic under-conductive layer, filling windows of the resist layer with a conductor by plating thereby forming a conductor layer, forming another windowed resist layer on the conductor layer and filling windows of this resist layer with a conductor by plating, thereby forming a via-hole layer and to provide a two-level structure of the conductor layer and the via-hole layer. Thereafter, the resist layers and portions of the metallic under-conductor layer other than those in contact with a lower face of the conductor constituting the conductor layer are dissolved to form a two-level skeleton structure of conductor lines and spaces within the skeleton structure are filled with a varnish in a solventless form and the varnish is cured.

64 Claims, 70 Drawing figures